IN THE CLAIMS

Please cancel claims 1-42 without prejudice or disclaimer.

1. - 42. (Canceled)

43. (Currently Amended) A timing circuit, comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal adapted to isolate a first memory array; and

an output connected to an address decoder adapted to address a second memory array, wherein the timing circuit activates the address decoder based on the at least one input signal.

44. (Original) The timing circuit according to claim 43, wherein the at least one input signal includes a RAS* signal.

45. (Original) The timing circuit according to claim 44, wherein the output activates the address decoder based on a low RAS* signal and a low isolation signal.

46. (Currently Amended) ~~The timing circuit according to claim 45,~~ A timing circuit, comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal;

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal; and

wherein the isolation signal is associated to a first memory array separate from a second memory array connected to the address decoder.

47. (Original) The timing circuit according to claim 43, wherein the input is connected to a NOR gate.

48. (Original) The timing circuit according to claim 43, wherein the input is connected to an AND gate.

49. (Previously Presented) A timing circuit connected to a wordline decoder of a first memory array, the timing circuit comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal connected to a sense amplifier for a second memory array; and

an output connected to the wordline decoder, wherein the timing circuit activates the wordline decoder based on the at least one input signal.

50. (Original) The timing circuit according to claim 49, wherein the at least one input signal includes a RAS* signal.

51. (Original) The timing circuit according to claim 50, wherein the output activates the wordline decoder based on a low RAS* signal and a low isolation signal.

52. (Original) The timing circuit according to claim 49, wherein the input is connected to a NOR gate.

53. (Original) The timing circuit according to claim 49, wherein the input is connected to an AND gate.

54. (Original) The timing circuit according to claim 49, wherein the first memory and the second memory array are connected to one sense amplifier.

55. (Withdrawn) A memory device comprising:

a plurality of memory cells coupled to digit lines;

a sense amplifier;

a plurality of isolation gates coupled between the sense amplifier and the digit lines, the isolation gates being controlled by isolation signals;

a timing circuit connected to one of the plurality of isolation gates; and

a wordline decoder connected to the timing circuit and at least one of the memory cells, wherein the timing circuit triggers the wordline decoder upon a state change in isolation signal at the one isolation gate.

56. (Withdrawn) The memory device according to claim 55, wherein the timing circuit is connected to a RAS* signal and activates the wordline decoder based on both the isolation signal and the RAS* signal shifting low.

57. (Withdrawn) The memory according to claim 56, wherein the isolation signal experiences a delay from its source to the isolation gate relative to the RAS* signal.

58. (Withdrawn) A memory device comprising:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

59. (Withdrawn) The memory device according to claim 58, wherein the first timing circuit receives a RAS* signal, and based on the RAS* signal and the state of the first isolation signal selectively activates the second wordline decoder.

60. (Withdrawn) The memory device according to claim 58, wherein the second isolation line transmits a second isolation signal to the second isolation gate, and a second timing circuit is connected to the second isolation line and the first wordline decoder and activates the first wordline decoder based on a change of state of the second isolation signal.

61. (Withdrawn) The memory device according to claim 60, wherein the second timing circuit receives a RAS* signal and based on the RAS* signal and the state of the second isolation signal selectively activates the first wordline decoder.

62. (Withdrawn) The memory device according to claim 60, wherein the plurality of sense amplifier banks includes N sense amplifier banks and N first isolation gates, plurality of memory arrays includes N * 2 memory arrays, and a number of first timing circuits equals N, and the number of second timing circuits is N.

63. (Withdrawn) The memory device according to claim 58, wherein the memory device is one of a DRAM, SRAM, Flash memory, SGRAM, SDRAM, SDRAM II, DDR SDRAM, Synchlink DRAM, and Rambus DRAM.

64. (Withdrawn) A computer, comprising:

a processor;

a plurality of memory arrays coupled to the processor, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

65. (Withdrawn) An integrated circuit, comprising:

a semiconductor wafer having first and second surfaces; and

a functional circuit formed on the first surface of the semiconductor wafer, the functional circuit including:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

66. (Withdrawn) An electronic system, comprising:

a processor; and

a memory coupled to the processor, the memory including:

a plurality of memory arrays, each memory array including a plurality of memory cells;

a plurality of sense amplifier banks, each of the sense amplifier banks including a first isolation gate, a second isolation gate, a first pair of digit lines connected to a first of the memory arrays, and a second pair of digit lines connected to a second of the memory arrays;

first and second isolation lines respectively connected to the first and second isolation gates of each of the plurality of sense amplifier banks, the first isolation line transmitting a first isolation signal to the first isolation gate;

first and second wordline decoders respectively connected to the first and second memory arrays; and

a first timing circuit connected to the first isolation line and the second wordline decoder, the first timing circuit activating the second wordline decoder based on a change of state of the first isolation signal.

67. (Withdrawn) The electronic system according to claim 66, wherein the processor includes a user interface device.

68. (Withdrawn) A method of reducing data corruption in a memory device, comprising:
providing a timing circuit in the memory device;
connecting a wordline decoder to a memory array;
linking activation of the wordline decoder to the timing circuit; and
producing a wordline activation signal from the timing circuit based on a nearby ISO signal.

69. (Withdrawn) The method of claim 68, wherein producing the wordline activation signal includes relying on the physical arrival of the ISO signal and not on an estimate of the arrival of the ISO signal.

70. (Currently Amended) An integrated circuit, comprising:
a memory array,
a plurality of sense amplifiers operably connected to the memory array,
an isolation gate operably connected between the memory array and the sense amplifiers, and
~~a~~ timing circuits ~~operable~~ operably connected to the isolation gate, comprising:

an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal; and

an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal.

71. (Withdrawn) A timing, integrated circuit, comprising:

an input adapted to receive a row access signal and a sense amplifier isolation signal; and

an output adapted to connect an address decoder, wherein the timing circuit activates the address decoder based on a state of the row access signal and the sense amplifier isolation signal.

72. (Withdrawn) The timing, integrated circuit according to claim 71, wherein the output presents an activation signal to the address decoder based on the row access signal being low and the sense amplifier isolation signal being low.

73. (Withdrawn) The timing, integrated circuit according to claim 72, wherein the input includes a NOR gate.

74. (Withdrawn) The timing, integrated circuit according to claim 72, wherein the input includes an AND gate.

75. (Withdrawn) An integrated circuit adapted to time activation of a wordline decoder to a sense amplifier isolation signal, comprising:

a first input connected to a sense amplifier isolation signal line;

a second input adapted to receive a memory access control signal;

an output adapted to activate/deactivate a wordline decoder based on the first input and the second input.

76. (Withdrawn) The integrated circuit of claim 75, wherein the second input receives a row access strobe signal.

77. (Withdrawn) The integrated circuit of claim 75, wherein the second input receives a low, active signal.

78. (Withdrawn) The integrated circuit of claim 75, further comprising a logic element that produces an output signal on the output based on the first input and the second input.

79. (Withdrawn) A timing circuit, comprising:

a delay circuit connected to a sense amplifier isolation signal line;

a first input connected to the delay circuit;

a second input adapted to receive at least one input signal; and

an output based on the first input and the second input and connected to an address decoder, wherein the timing circuit activates the address decoder based on the first input signal and the second input signal.

80. (Withdrawn) The timing circuit of claim 79, wherein the delay circuit includes a programmable delay.

81. (Withdrawn) The timing circuit of claim 80, wherein the programmable delay is within a range of programmable delay times.

82. (Withdrawn) The timing circuit of claim 81, wherein the range of programmable delay times represents the propagation time of a sense amplifier isolation signal on the sense amplifier signal line.

83. (Withdrawn) timing circuit of claim 79, wherein the delay circuit is adapted to produce a delay based on a propagation time of an isolation signal.

84. (Withdrawn) The timing circuit of claim 79, wherein the delay circuit is adapted to produce a delay based on a signal required for accessing a wordline, column or memory location in a memory device.

85. (Withdrawn) An integrated circuit adapted to time activation of a wordline decoder to a sense amplifier isolation signal, comprising:

a first input adapted to receive a sense amplifier isolation signal;

a second input adapted to receive a memory access control signal;

a timing output adapted to activate/deactivate a wordline decoder based on the first input and the second input.

86. (Withdrawn) The integrated circuit of claim 85, wherein the first input is active, the second input is inactive and the timing output is inactive.

87. (Withdrawn) The integrated circuit of claim 86, wherein the first input is active at a high state and the second input is active at a low state.

88. (Withdrawn) The integrated circuit of claim 85, wherein the timing output produces an active signal with the first input being low and the second input being low.

Please add the following:

89. (New) The timing circuit according to claim 46, wherein the at least one input signal includes a RAS* signal.

90. (New) The timing circuit according to claim 46, wherein the output activates the address decoder based on a low RAS* signal and a low isolation signal.

91. (New) The timing circuit according to claim 46, wherein the input is connected to a NOR gate.

92. (New) The timing circuit according to claim 46, wherein the input is connected to an AND gate.

REMARKS

This paper replaces the response to the final office action mailed to the USPTO on May 5, 2003, which response was not entered and should not be entered.

Claims 43, 46, and 70 are amended, claims 1-42 are canceled, and claims 89-92 are added; as a result, claims 43-92 are now pending in this application.

Applicant cancels method claims 1-42 without prejudice or disclaimer. Applicant intends to file a divisional application directed to these claims.

Election/Restriction

Applicant respectfully requests consideration of claims 70-88. For example, claim 70 recites, in part, an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal; and an output connected to an address decoder, wherein the timing circuit activates the address decoder based on the at least one input signal. This is essentially the same subject matter as claim 43. Accordingly, if claim 43 is found allowable, then claim 70 is also allowable. Claim 71 should also be considered. Claim 71 includes, in part, the similar subject matter as found in claim 43. If claim 43 is found allowable, then claims 71-74 are also allowable. Applicant submits that consideration of claims 70-88 would not place additional burdens on the examiner. Reconsideration of the assertion of constructive election is requested.

§103 Rejection of the Claims

Claims 43-54 were rejected under 35 USC § 103(a) as being unpatentable over Butler et al. (U.S. Patent No. 5,392,241) in view of Uruma et al. (U.S. Patent No. 5,313,431). Applicant respectfully traverses.

Claim 43 recites, in part, "an input adapted to receive at least one input signal, the at least one input signal including a sense amplifier isolation signal adapted to isolate a first memory array." Applicant can not find this feature in Butler or Uruma. Reconsideration is requested.

The Office Action cites col. 7, lines 12-15 of Butler as teaching the immediately-above feature of claim 43. Col. 7, lines 12-15 of Butler recites "Sense amplifier timing chain 80 also receives input from an address decode circuit 82, which itself is controlled by row/column addresses received from controller 74." This portion of Butler clearly lacks any specific reference to a sense amplifier signal as recited in claim 43.

Claim 43 further recites, in part, "an output connected to an address decoder adapted to address a second memory array, wherein the timing circuit activates the address decoder based on the at least one input signal." Applicant can not find this feature in Butler or Uruma. Reconsideration is requested.

The Office Action cites col. 7, lines 15-24 of Butler as teaching the immediately-above feature of claim 43. Col. 7, lines 15-24 of Butler recites

> Timing chain 80 outputs SETBL and SETBLN signals, along with their compliments, to primary and secondary set devices of memory array 76. One of ordinary skill in the art can readily implement a timing chain to provide these signals, which are depicted and described herein. Also output from address decoder 82 are word line address signal "WL" and write switching signal "Y". An I/O interface 84 receives/-transmits data between memory circuit 72 and controller 74, and is coupled to memory array 76.

This portion of Butler clearly lacks any specific reference to a timing circuit that includes an output connected to an address decoder that is adapted to address a second memory array. Moreover, this portion of Butler clearly lacks any specific reference to the timing circuit activating the address decoder, which is adapted to address a second memory array, based on the at least one input signal, which is adapted to isolate a first memory array, as recited in claim 43.

The Office Action states that although not expressly stated as such, the sense amp timing chain 80, upon receiving an input, causes activation of the address decoder. Applicant respectfully traverses this assertion. First, the timing chain 80 receives input from the address decoder. The address decoder 82 must be active to send a signal to the timing chain 80. Applicant can not find any disclosure in Butler that states any activation dependence of the address decoder 82 on the timing chain 80. Second, applicant submits that Butler teaches away from the present invention as recited in claim 43. Specifically,

Butler states that the sense amplifier timing chain 80 receives input from the address decode circuit 82. Applicant does not see how the timing amplifier chain 80 can activate the address decoder if the address decoder provides the input to the timing amplifier chain 80.

As applicant can not find a timing circuit in Butler that includes an input adapted to receive a sense amplifier signal or an output connected to the address decoder as recited in claim 43, applicant submits that claims 43-45 and 47-48 are allowable.

Applicant requests clarification of the present rejection as the Office Action simultaneously indicates that claim 46 is rejected as obvious and is allowable.

Applicant requests clarification of the present obviousness rejection, which is a combination of Butler and Uruma. The Office Action at pages 3 and 4 discusses Butler as teaching elements of claims 43-54. There is no discussion of Uruma or how one of skill in the art would be motivated to combine Butler with Uruma to reject claims 43-53. Clarification is required for appeal.

Claim 49 is believed to be allowable for substantially similar reasons as stated above with regard to claim 43. Moreover, claim 49 is similar to claim 46, which was indicated as allowable. Reconsideration of claim 49 and its dependent claims 50-54 is requested.

The Examiner appears to reject claims 43-53 based only on Butler. Applicant respectfully traverses the single reference rejection under 35 U.S.C. § 103 since not all of the recited elements of the claims are found Butler. Since all the elements of the claim are not found in the reference, Applicant assumes that the Examiner is taking official notice of the missing elements. Applicant respectfully objects to the taking of official notice with a single reference obviousness rejection and, pursuant to M.P.E.P. § 2144.03, Applicant respectfully traverses the assertion of Official Notice and requests that the Examiner cite references in support of this position.

The Office Action took official notice of the "limitations" of claims 44-45, 47-48, and 50-53. Applicant respectfully traverses this official notice and requests the Examiner to provide a reference that describes such an element. Absent a reference, it appears that the Examiner is using personal knowledge, so the Examiner is respectfully requested to submit an affidavit as required by 37 C.F.R. § 1.104(d)(2).

Claim 54 was rejected under 35 USC § 103(a) as being unpatentable over Butler et al. in view of Uruma et al. Applicant traverses for at least the reasons stated above with regard to claim 49.

Allowable Subject Matter

Claim 46 was objected to as being dependent upon a rejected base claim, but was indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 46 is so rewritten. Allowance of claim 46 is requested. New claims 89-92 depend from claim 46 and are believed to be allowable therewith.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Name

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